# AD9361 DCXO User Guide

# TABLE OF CONTENTS



### REVISION HISTORY

**10/2011—2.0** Release

**7/2012—2.1** Added important note regarding DCXO temperature compensation

# GENERAL DESCRIPTION

The AD9361 uses fractional-n phase locked loops (PLLs) to generate the transmitter and receiver local oscillator (LO) frequencies as well as the oscillator (the baseband PLL) used for the data converters, digital filters, and I/O port. These PLLs all require a reference clock input, which can be provided by an external oscillator or by an external crystal (XO) and a digitally programmable on-chip variable capacitor. The capacitor fine-tunes the resulting reference clock frequency. This combination of XO and trimming capacitor is collectively referred to as the DCXO.

Applications such as wireless basestations require that the reference clock lock to a system master clock. In these situations, an external oscillator such as a VCTCXO should be used in conjunction with a synchronizing PLL such as the AD9548. Wireless user equipment (UE), however, do not typically need to be locked to a master clock but they do need to adjust the LO frequency periodically to maintain connection with a basestation. The basestation (BTS) occasionally informs the UE of its frequency error relative to the BTS. By adjusting the trimming capacitor, the baseband processor can adjust the reference clock frequency and thus the LO frequency as needed.

The RFPLLs and the BBPLL should maintain minimal frequency drift with temperature. However, typical XOs have an "S" curve response of frequency vs. temperature, making it more difficult for a baseband processor to correct the frequency error at startup and during operation.

This document describes the setup and operation of the DCXO as well as a method of on-chip DCXO temperature compensation that can reduce temperature-induced frequency error to within a few ppm.

# DCXO SETUP AND OPERATION

To use the DCXO, connect an external crystal (XO) between the XTALP and XTALN pins of the AD9361. Valid crystal resonant frequencies range from 19MHz to 50MHz. The crystal must be an AT cut fundamental mode of vibration with a load capacitance of 10pF.

By adjusting a capacitor within the AD9361, the resulting DCXO frequency can be adjusted to compensate for XO frequency tolerance and stability. Register 0x292[D5:D0] sets a coarse capacitor value while registers 0x293[D7:D0] and 0x294[D7:D3] set a fine capacitor value. Together, these three registers control the frequency of the DCXO. The resolution of the DCXO varies with coarse word with a worst case resolution (at coarse word = 0) of 0.0125 ppm. Using both coarse and fine words, the DCXO can vary the frequency over a ±60 ppm range.

Using a bench test, nominal DCXO trimming words in 0x292 through 0x294 should be determined and then used in an initialization script. These nominal words should be written before the AD9361 BBPLL is calibrated. After initialization (after the BBPLL and RFPLLs are programmed, calibrated, and locked), the DCXO words may be written at any time.

The plot below shows the variation of DCXO frequency over all possible variations of coarse and fine word. The XO nominal frequency used in this test was 40MHz.

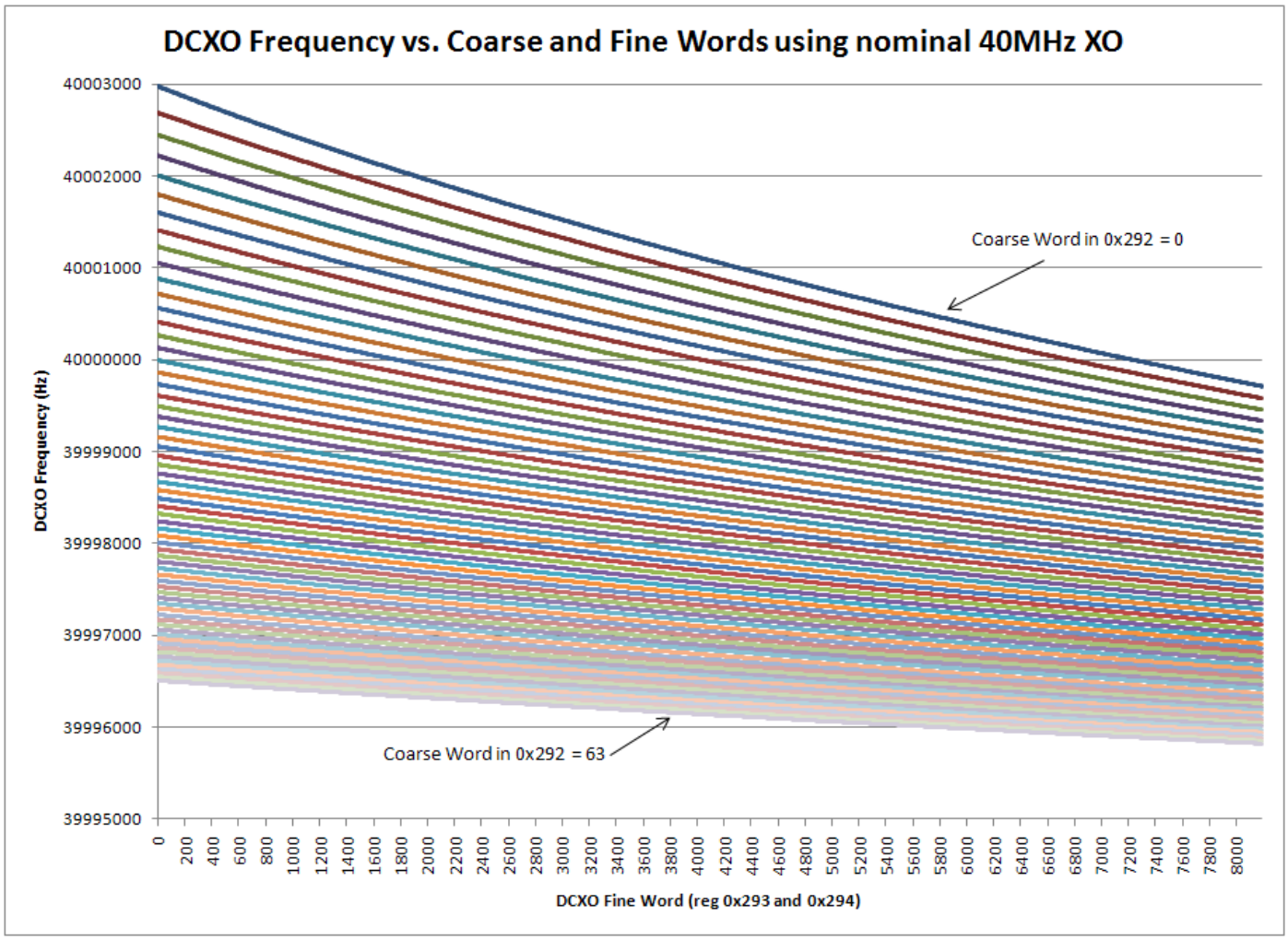


Figure 1. DCXO Frequency vs Coarse and Fine Words

The AD9361 Rx and Tx RFPLLs use the DCXO as a reference clock input. For this reason, it is extremely critical that the DCXO have very low phase noise. The AD9361 evaluation board using the DCXO with an external Epson Toyocom crystal has excellent phase noise performance, resulting in excellent EVM performance as well. The DCXO phase noise performance is shown in the plot below. Any other external crystal choice should first be measured in the DCXO circuit and compared against the plot below.

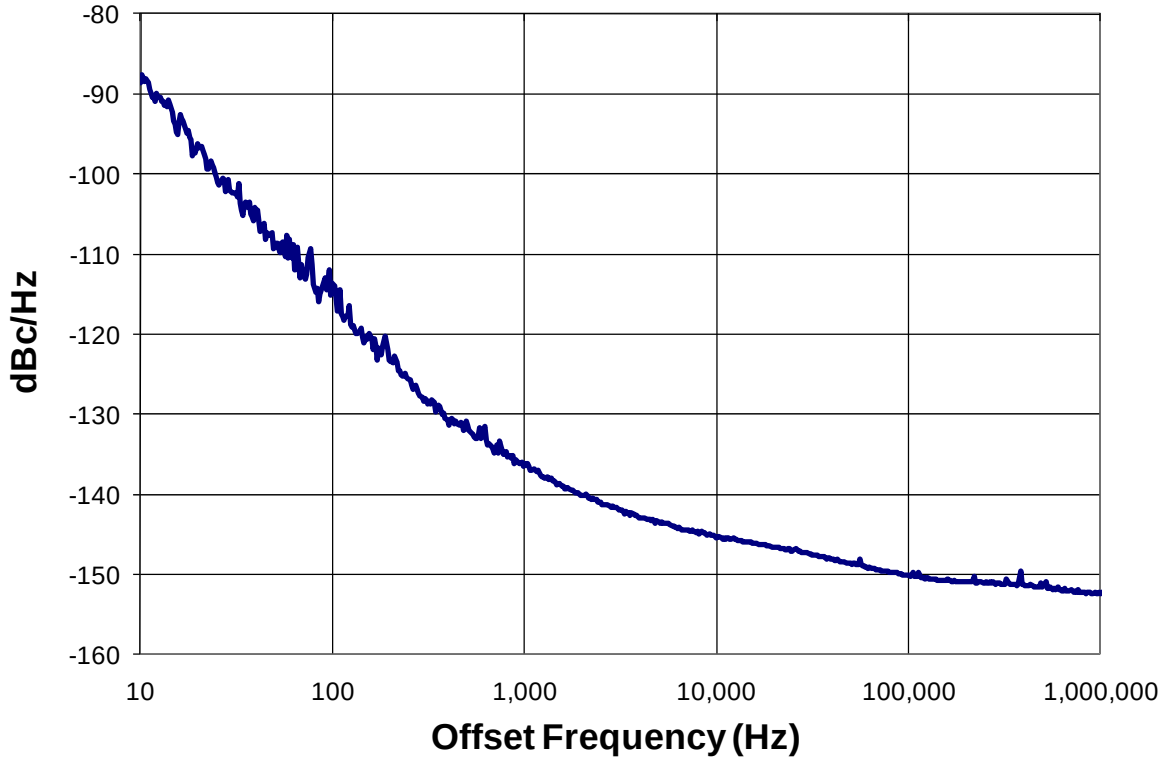


Figure 2. DCXO Phase Noise vs Offset Frequency

# DCXO TEMPERATURE COMPENSATION

**Important Note:** In the DCXO temperature compensation algorithm, values are determined by bench testing and a table is created and then input into the AD9361 in the field. However, the values used in the table are divided by 16 which reduces the accuracy of the algorithm. This inaccuracy is then multiplied up to the RF LO frequency. For this reason, the temperature compensation function has limited use with LO frequencies above 1GHz. For LO frequencies below 1GHz, the potential performance of the algorithm should be evaluated against the system requirements before assuming that the function will provide the required benefit.

External crystal frequency typically varies with temperature according to a third order equation. The equation varies with several factors including the cut angle of the crystal. This non-monotonic "S" curve behavior can make it more difficult for a BBP to change its LO frequency to match the basestation LO frequency.

DCXO temperature compensation first requires a system to be characterized once for DCXO frequency variation vs. temperature. This is typically a bench test performed on the final product in its final enclosure, not a factory test performed on every unit. At each temperature, the DCXO fine-tune word is changed such that the resulting DCXO frequency is the same as the nominal DCXO frequency. The test creates a matrix of temperature vs. DCXO correction word and this matrix is stored in system non-volatile memory. During initialization in the field, the matrix is programmed into an internal table in the AD9361. Setting a bit causes the AD9361 to measure its internal temperature which recalls an internal table entry of the DCXO correction word. This word adds to the nominal DCXO fine-tune word. Expected DCXO tracking is within a couple of ppm.

Note: The bench test and operation of DCXO correction require setting the "Force Temp Sensor for Cal" bit in 0x147. The Gain Step Calibration (if it is performed as part of a factory test) must have this bit cleared. Thus, to run a Gain Step Calibration make sure to clear this bit.

## ONE-TIME TEMPERATURE VS. FREQUENCY VARIATION BENCH TEST

The sequence of steps below describes how to perform the one-time (bench) characterization routine.

1. Place the complete product (including case, all circuit boards, etc.) into a temperature chamber. Naturally, this would also include the AD9361 and the external XO. Set the temperature to a nominal value.

2. Initialize the system, put it into the desired operating mode, and wait for the temperature to stabilize. Most importantly, make sure that the XO temperature stabilizes.
    a. Configure the temperature sensor
        i. Enable the sensor by setting bit D0 in 0x00D.
        ii. Use a large decimation factor such as 16k or 32k (0x00F = 3'b110 or 3'b111).
        iii. Set the temperature sensor update interval l time to be long (such as 10 seconds). Setting this interval time in register 0x00D depends on the BBPLL rate but in general, an interval value of 7'b0001100 is a good start. With bit D0 set in step (i), 0x00D would then equal 0x19.
    b. If using a frequency counter to check the DCXO frequency, make sure that CLK_OUT is enabled in 0x00A and with bits D7-D5 = 3'b000 so that a buffered version of the DCXO is present on CLK_OUT. 0x00A also controls the BBPLL post-dividers so make sure to first read 0x00A and then change only bits D7-D4.
3. Set the "Force Temp Sensor for Cal" bit in 0x147[D6]. This bit forces the calibration routine to use the value in 0x149 as the nominal temperature word.
4. Read the temperature word in register 0x00E and write that value into the "Cal Temp Sense Word" of 0x149. Also store this word in non-volatile memory in the system. This will be the reference temperature word at "nominal" temperature.
5. At this nominal temperature, set the DCXO fine and coarse words such that the DCXO is at the desired frequency (within 1 Hz) and store the correction word.
6. Sweep temperature over the full expected ambient temperature range of the system in 4 degree steps. At each step,
    a. Change the temperature and let the system reach temperature equilibrium
    b. Read the "Delta T Read Back" Register 0x299, divide the value by 4 and record the quotient
    c. Adjust the DCXO fine word to bring the DCXO back to the desired frequency within 1 Hz and record this word. Subtract the DCXO fine word at nominal from this new value, divide the result by 16, and convert to a 2's complement 8-bit word. Record this delta DCXO fine word.
7. The result will resemble Table 1. In this table, the nominal temperature was 24 degrees C and the sweep ranged from -40 degrees C to +88 degrees C. The "Delta Temperature Word" in 0x299 is offset binary so a value of 0x80 represents a delta temperature of zero. Dividing 0x299 by 4 results in a value of 0x20 at nominal temperature. Absolute temperature and delta temperature in degrees C are not used by the AD9361 but are shown in the table for clarity. The maximum sweep range (limited by the correction table size) is +127/-128 degrees from nominal.
8. Table 1 is now holds information showing how to compensate the DCXO fine word for different system temperatures. However, this information corresponds to only one sample of the crystal. For maximum accuracy, this same characterization should be performed over the expected process variation of the crystal. An average of the DCXO fine delta words would be used as the final table. These tests would be completed prior to mass production.
9. This ends the bench characterization testing. The right-most two columns of the table must be stored in the BBP so that they can be loaded into the AD9361 when it is initialized in the field. The temperature word at nominal temperature determined in step 4 above must be stored as well.

| Absolute Temp (degrees C) | Delta T (degrees C) | Delta Temperature Word in 0x299divided by 4 (hex) | Delta DCXO Correction Word (example) divided by 16 and converted to 2's complement (8 bits) (hex) |
|---|---|---|---|
| 88 | 64 | 30 | 0D |
| 84 | 60 | 2F | 14 |
| 80 | 56 | 2E | 20 |
| 76 | 52 | 2D | 1B |
| … | | | |
| 24 | 0 | 20 | 0 |
| … | | | |
| -28 | -52 | 13 | E5 |
| -32 | -56 | 12 | E3 |
| -36 | -60 | 11 | E1 |
| -40 | -64 | 10 | E4 |

Table 1. Initial Results of Temperature Sweep

# FACTORY TESTING

The object of the temperature compensation algorithm is to compensate for temperature variation. However, even at the same temperature, all crystals will have slightly different resonance frequencies. All systems should undergo a single-point factory test in which the temperature is some nominal value and the DCXO fine word needed to bring the DCXO frequency to the desired frequency is recorded. This will be the reference fine word that the BBP will use to get the DCXO to the nominal frequency.

# AD9361 INITIALIZATION IN THE FIELD

Once the system is in the field, the matrix created by the bench testing steps is programmed into a lookup table in the AD9361. This occurs during the initialization routine once, when the system is powered up.

1. Set the "Force Temp Sensor for Cal" bit in 0x147[D6].
2. Write the temperature word stored in non-volatile memory into register 0x149. See step 4 of the bench testing sequence above where this value was determined.
3. Write the nominal DCXO fine word into registers 0x293 and 0x294.
4. Program the DCXO Correction Words stored in non-volatile memory into the Lookup Table. For each row of table 1,
    a. Write the value in the right-most column into 0x296. This is the "data" at this table entry.
    b. Write the Delta Temperature Word divided by 4 into 0x298[D5:D0]. This is the "address" of the table entry.
    c. Set the DCXO Tempco Clk bit high at (0x298[D6] in addition to re-writing the address in bits D5:D0. This writes the data into the table at the address specified by 0x298[D5:D0].
    d. Clear the DCXO Tempco Clk bit
    e. Repeat for all table entries

# OPERATION

Set bit D7 of 0x298 to enable temperature compensation. The "Force Temp Sensor for Cal" bit in 0x147[D6] must still be set.

The compensation circuit will continuously monitor the temperature of the AD9361 using the temperature sensor. It will determine the delta temperature word by subtracting the current word from the nominal word in 0x149. The AD9361 will divide this delta by 4, resulting in the table address. The DCXO correction word (from the right-most column in Table 1) at this address is added to the MSBs of the DCXO fine word.. This will bring the DCXO frequency back to the desired value, essentially negating the temperature dependence of the crystal.

If the delta temperature word divided by 4 is not exactly equal to the address of a table entry, the algorithm interpolates between two table entries to determine the correct DCXO correction word.

Typically, during operation the BTS periodically informs the UE of any frequency delta between the two stations. Changing the DCXO fine word to remove that frequency error is completely compatible with the temperature compensation circuit.